LISTING OF CLAIMS

Claim 1 (Withdrawn): A motherboard comprising:

a video display port;

a reprogrammable non-volatile memory;

a controller for said non-volatile memory;

a graphics controller circuit for outputting video signals; and

a wired-OR circuit connecting said graphics controller circuit to said controller to said port.

Claim 2 (Withdrawn): The motherboard of claim 1 wherein said non-volatile memory is flash memory.

Claim 3 (Withdrawn): The motherboard of claim 2 further comprising:

a microprocessor;

a main memory; and wherein said flash memory for storing BIOS and controller firmware.

Claim 4 (Withdrawn): The motherboard of claim 3 wherein said controller is connected to said wired-OR circuit by a serial programming interface.

Claim 5 (Withdrawn): The motherboard of claim 4 wherein said graphics controller is connected to said wired-OR circuit.

Claim 6 (Withdrawn): The motherboard of claim 5 wherein said wired-OR circuit further comprises: the VGA port circuit and the non-volatile memory serial programming interface circuit.

Claim 7 (Withdrawn): A computer system comprising:

a peripheral device;

a system board coupled to the peripheral device, the system board comprising:

a processor;

a main memory;

a video port;

a graphics controller circuit;

a non-volatile memory;

a controller for said non-volatile memory; and

means for connecting said graphics controller circuit to said controller and to said video port permitting signals from said graphics controller to be outputted to said video port, and permitting signals from said video port to be supplied to said controller to program said non-volatile memory.

Claim 8 (Withdrawn): The computer system of claim 7 wherein said non-volatile memory is flash memory.

Claim 9 (Withdrawn): The computer system of claim 8 wherein said flash memory for storing BIOS and firmware for said controller.

Claim 10 (Withdrawn): The computer system of claim 9 wherein said connecting means is a wired-OR circuit.

Claim 11 (Withdrawn): The computer system of claim 10 further comprising a serial programming interface, and wherein said controller is connected to said wired-OR circuit through said serial programming interface.

Claim 12 (Withdrawn): The computer system of claim 11 wherein said graphics controller circuit is connected to said video port by said wired-OR circuit.

Claim 13 (Withdrawn): The computer system of claim 7 further comprising a plurality of peripheral devices, wherein each peripheral device has an associated peripheral controller, and

wherein each peripheral controller having an associated non-volatile memory and an associated serial programming interface, having a unique address.

Claim 14 (Withdrawn): The computer system of claim 13 wherein said serial programming interface associated with each peripheral controller are all connected together to said video, permitting signals from said video port to be supplied to an addressed peripheral controller to program the associated non-volatile memory.

Claim 15 (Original): A non-volatile memory device comprising:

an array of non-volatile memory cells;

a first port for receiving a first communication protocol and for interfacing with said array in said first communication protocol; and

a second port for receiving a second communication protocol and for converting said second communication protocol into said first communication protocol.

Claim 16 (Original) : The non-volatile memory device of claim 15 wherein said first communication protocol is a superset of said second communication protocol.

Claim 17 (Original) : The non-volatile memory device of claim 15 further comprising a circuit for detecting a sequence of signals supplied at said second port and for switching communication from said first port to said second port.

Claim 18 (Original) : The non-volatile memory device of claim 16 wherein said first communication protocol is in accordance with the LPC protocol.

Claim 19 (Original) : The non-volatile memory device of claim 18 wherein said second communication protocol transmits each nibble-wise field of the LPC bus protocol with four clock pulses.

Claim 20 (Original) : The non-volatile memory device of claim 19 wherein said second communication protocol receives three signals: a clock signal, a data/command signal, and a control signal.